DATABASE

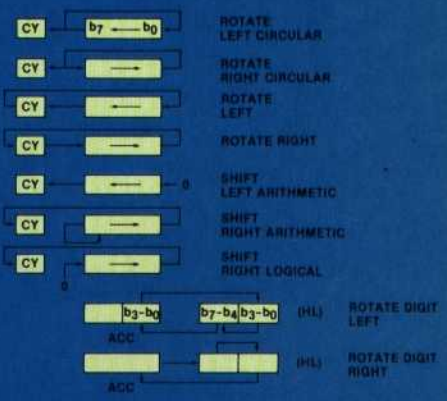
Here, courtesy of Zilog Inc, we reproduce a further part of the Z80 programmers' reference card

Rotate and Shift Group

SOURCE AND DESTINATION

TYPE OF ROTATE OR SHIFT	A	B	C	D	E	H	L	(HL)	(IX + d)	(IY + d)
'RLC'	CB 07	CB 00	CB 01	CB 02	CB 03	CB 04	CB 05	CB 06	DD CB d 06	FD CB d 06
'RRC'	CB 0F	CB 08	CB 09	CB 0A	CB 0B	CB 0C	CB 0D	CB 0E	DD CB d 0E	FD CB d 0E
'RL'	CB 17	CB 10	CB 11	CB 12	CB 13	CB 14	CB 15	CB 16	DD CB d 16	FD CB d 16
'RR'	CB 1F	CB 18	CB 19	CB 1A	CB 1B	CB 1C	CB 1D	CB 1E	DD CB d 1E	FD CB d 1E
'SLA'	CB 27	CB 20	CB 21	CB 22	CB 23	CB 24	CB 25	CB 26	DD CB d 26	FD CB d 26
'SRA'	CB 2F	CB 28	CB 29	CB 2A	CB 2B	CB 2C	CB 2D	CB 2E	DD CB d 2E	FD CB d 2E
'SRL'	CB 3F	CB 38	CB 39	CB 3A	CB 3B	CB 3C	CB 3D	CB 3E	DD CB d 3E	FD CB d 3E
'RLD'								ED 6F		
'RRD'								ED 67		

	A
'RLCA'	07
'RRCA'	0F
'RLA'	17
'RRA'	1F



Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA	CY ← 7 ← 0 (A)	*	*	X	0	X	*	0	0	00 000 111	07	1	1	4	Rotate left circular accumulator
RLA	CY ← 7 ← 0 (A)	*	*	X	0	X	*	0	0	00 010 111	17	1	1	4	Rotate left accumulator
RRCA	7 → 0 → CY (A)	*	*	X	0	X	*	0	0	00 001 111	0F	1	1	4	Rotate right circular accumulator
RRA	7 → 0 → CY (A)	*	*	X	0	X	*	0	0	00 011 111	1F	1	1	4	Rotate right accumulator
RLC r		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 r	CB	2	2	8	Rotate left circular register r
RLC (HL)		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 110	CB	2	4	15	r: Reg 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (IX + d)	CY ← 7 ← 0 (IX + d)	↕	↕	X	0	X	P	0	↕	11 011 101 11 001 011 – d – 00 000 110	DD CB	4	6	23	
RLC (IY + d)		↕	↕	X	0	X	P	0	↕	11 111 101 11 001 011 – d – 00 000 110	FD CB	4	6	23	
RL m	CY ← 7 ← 0 m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	010					Instruction format and states are as shown for RLC s. To form new opcode replace 000 of RLC s with shown code
RRC m	7 → 0 → CY m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	001					
RR m	7 → 0 → CY m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	011					
SLA m	CY ← 7 ← 0 m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	100					
SRA m	7 → 0 → CY m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	101					
SRL m	0 → 7 → 0 → CY m = r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	111					
RLD	7–4 3–0 (A) 7–4 3–0 (HL)	↕	↕	X	0	X	P	0	*	11 101 101 01 101 111	ED 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL). The contents of the upper half of the accumulator is unaffected.
RRD	7–4 3–0 (A) 7–4 3–0 (HL)	↕	↕	X	0	X	P	0	*	11 101 101 01 100 111	ED 67	2	5	18	

NOTES: s represents the expression of the relative addressing mode
e is a signed two's complement number in the range < –126, 129 >
e-2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e

Flag Notation: * = flag not affected, 0 = flag reset, 1 = flag set, X = flag is unknown,
↕ = flag is affected according to the result of the operation.