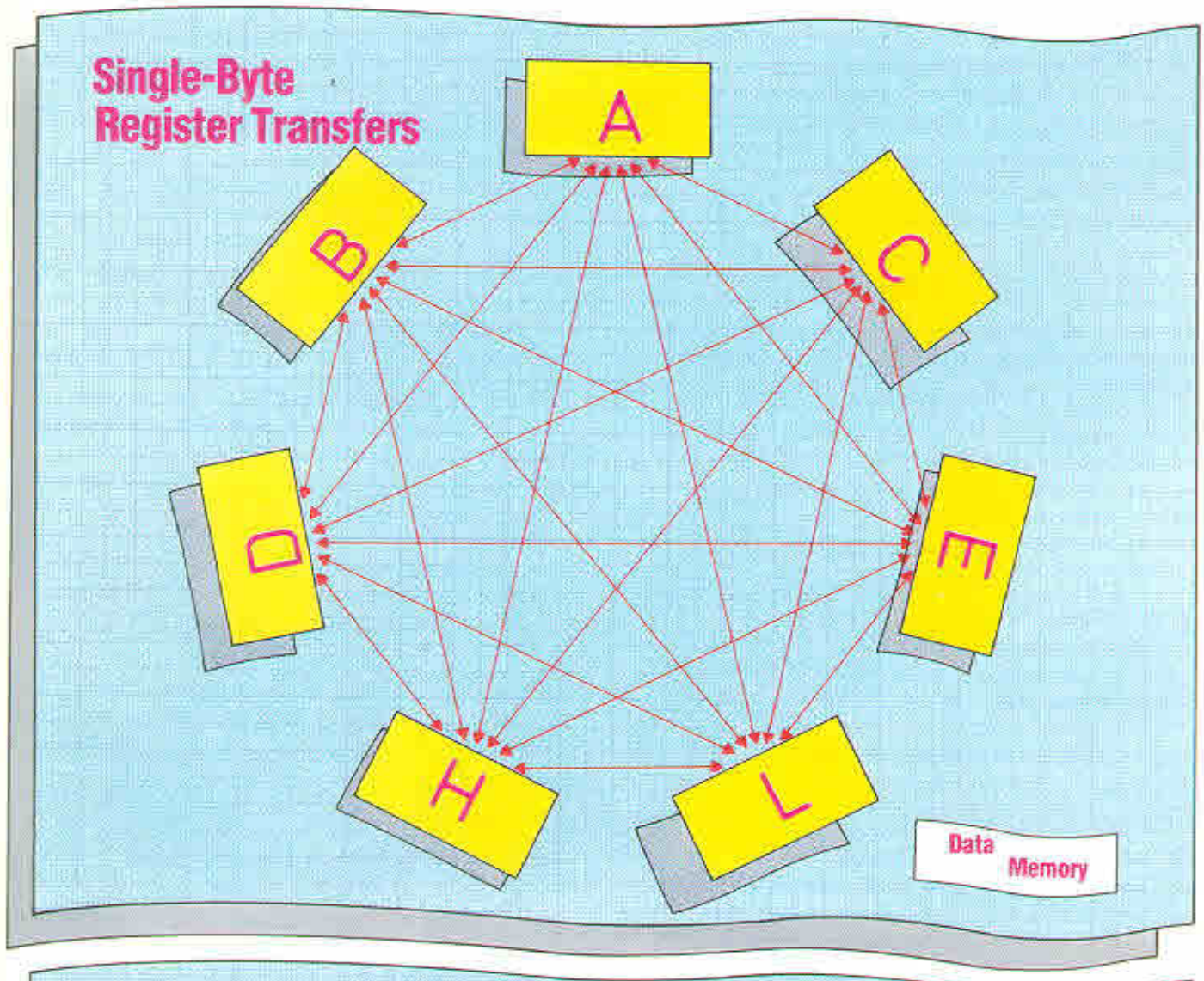

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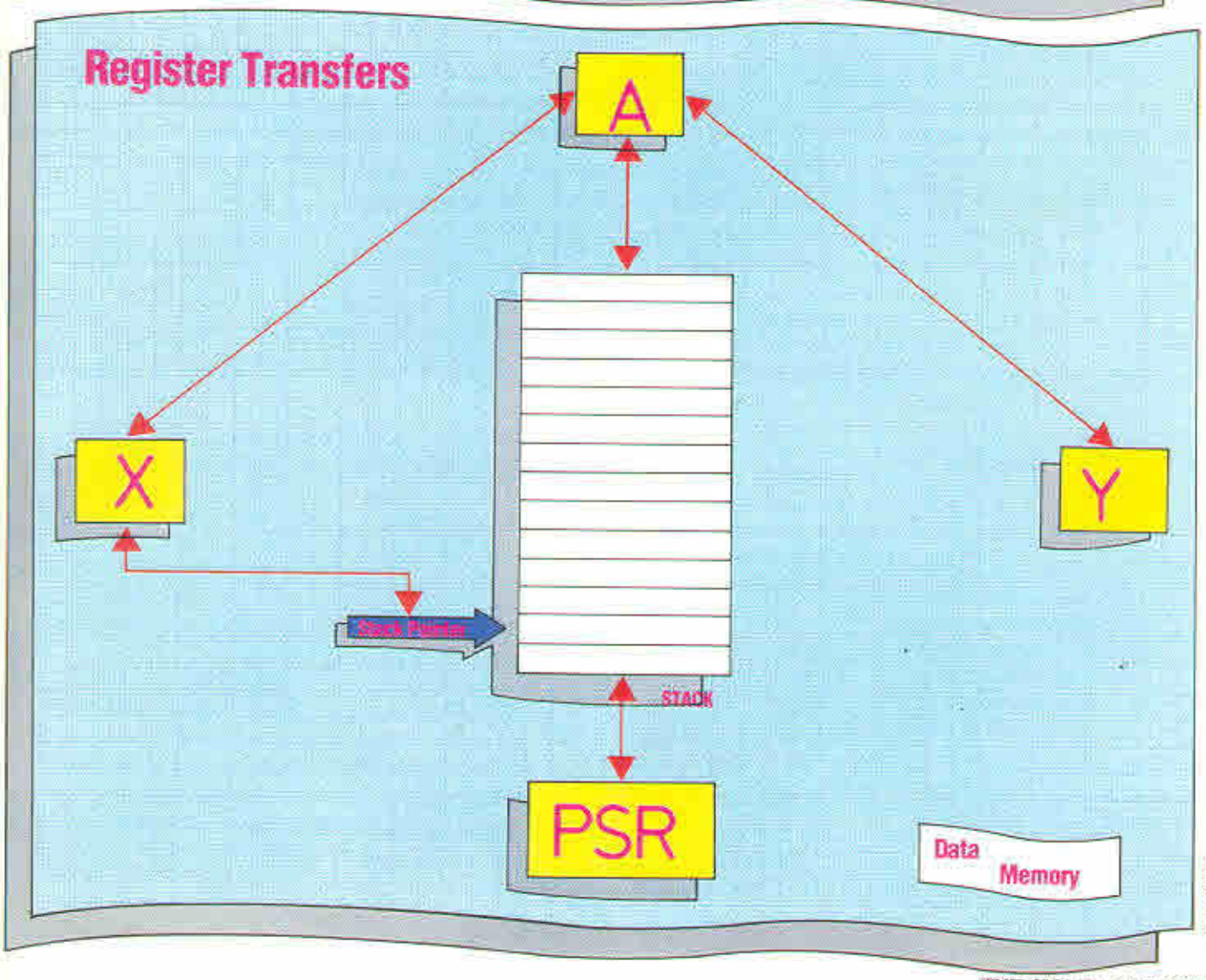
Double Identity
The Z80's data registers can communicate as single-byte registers with every other single-byte register. They can each communicate with memory in direct, immediate, indirect, absolute, and indexed modes. When treated as BC, DE, HL – the two-byte register pairs – they can transfer 16-bit data to and from memory and the stack, and are effectively 16-bit accumulators for addition and subtraction. This combination of flexibility and resourcefulness is the key to the Z80's huge success



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Plain And Simple
The 6502's internal communication is severely linear, and restricted to eight-bit data transfers. Only the accumulator can communicate directly with X and Y; only X can communicate with the stack pointer; and only the PSR and the accumulator access the stack. Memory transfers are possible in absolute, direct, indirect, indexed, immediate, and zero page modes. The 6502's inventive use of zero page mode compensates for the small size of its register set: zero page can be treated as 128 two-byte CPU registers