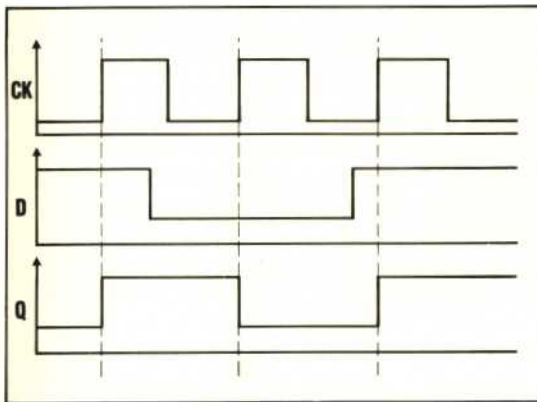
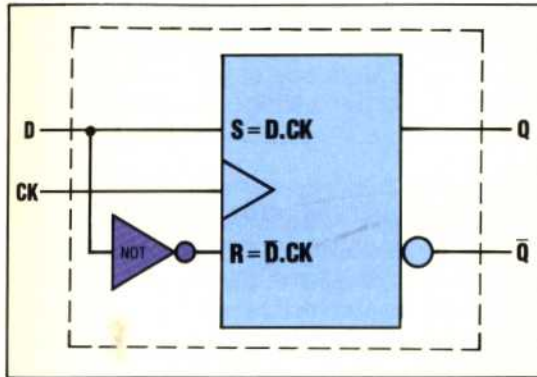




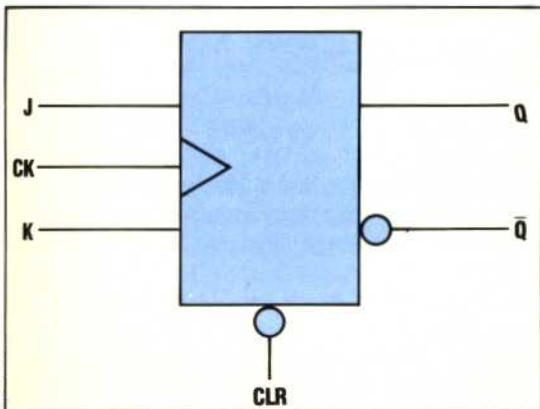
HI. If, however, the input at D is LO, then the output Q is set LO.



It can be seen from these graphs that the output Q can only change during a LO to HI transition of the clock. Consequently, the D-type is called a 'leading edge triggered' flip-flop.

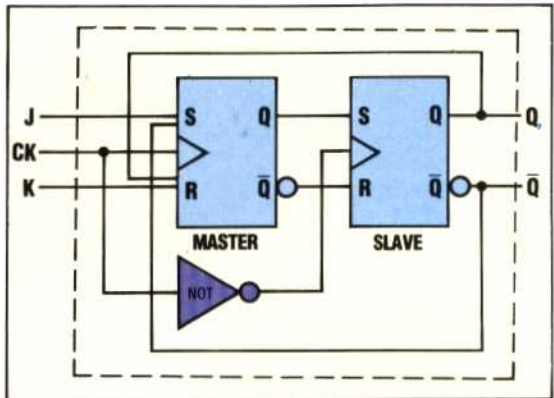
THE J-K FLIP-FLOP

The J-K flip-flop is known as a master-slave device as it comprises, in effect, two R-S flip-flops in a dominant-submissive relationship. A master-slave device allows an input pulse to be stored in one flip-flop, whilst simultaneously giving an output from the other unit dependent on the previous input, all within one clock cycle. An example of this is the shift operation common to most processors, where bits within the register are moved one place to the left or right. Here is the standard circuit diagram for a J-K flip-flop:



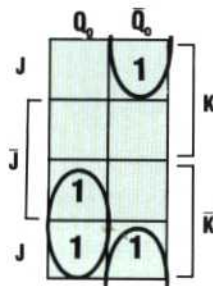
The following diagram shows how the two R-S types are linked together. One is the 'master' and

the other the 'slave'. Suppose an input is applied at J or K: if the clock pulse is HI then the input is fed to the master, if the clock input is LO then the slave inputs are fed, since R-S types are leading edge triggered. Thus only one R-S type is activated at any one time, with the previous input being 'locked' inside the other:



In the margin we give a *state table* for the J-K flip-flop. This is similar to a truth table but makes use of a variable, Q_0 , the previous output. Notice that HI inputs simultaneously at J and K cause the flip-flop to change state with each clock pulse. This is known as *toggling* and is caused by the feedback of the slave outputs to the master inputs. With an R-S flip-flop this is a disallowed input combination and the output is undefined. By considering Q_0, J and K as inputs, the results from the state table can be placed onto a k-map.

Q_0	J	K	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



From the k-map we can obtain a logic expression:

$$Q = Q_0 \cdot J + Q_0 \cdot K$$

This equation is known as the *characteristic* of the J-K flip-flop.

Answers To Exercise 7 On Page 229

- 1) A flip-flop is also known as a bistable because it is only stable in one of two states (namely, when $Q=1$ and $\bar{Q}=0$ or when $Q=0$ and $\bar{Q}=1$).
- 2) a) This is not a stable state.
 b) The flip-flop will change to the RESET state if the upper input is considered first, or the SET state if the lower gate is considered first.
 c) Yes (see answer to b).
 d) In order to make all the registers attain a predictable state on power-up they must be either reset or set during the initialising of the computer system.

Erratum

In the diagram of a full adder circuit on page 165 in Issue 9 the annotation was incorrect. The 'sum' and 'carry' labels should be interchanged on each half adder and in the final output. The caption is correct