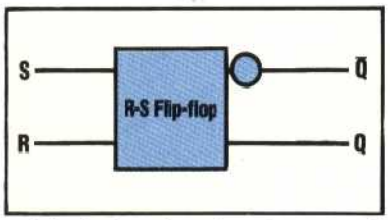
# SET PIECE

**The circuits that we have so far considered in the Logic course all produce given outputs upon receiving certain input signals. Sequential circuits, on the other hand, are capable of producing a steady output signal in response to a single input pulse. We examine in detail the design and function of such a circuit — the R-S flip-flop.**

Several kinds of flip-flop exist, although all of them operate from the same principles. The R-S flip-flop has two input and two output lines.

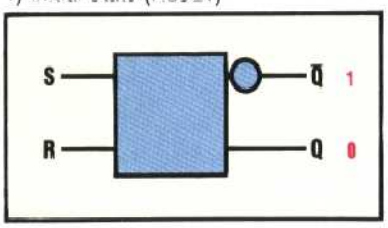



The circuit is designed so that the output lines, Q and $\overline{Q}$, are always opposite to each other. That is:

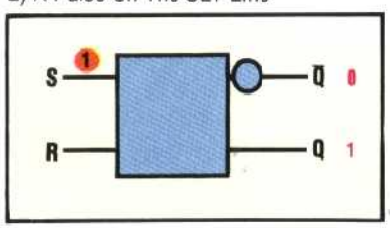
if Q = 1 then $\overline{Q}$ = 0 (the SET state)
if Q = 0 then $\overline{Q}$ = 1 (the RESET state)

Assuming that the flip-flop is initially in the RESET state, then a pulse on the S line causes the circuit to 'flip' over to the SET state.

1) Initial State (RESET)

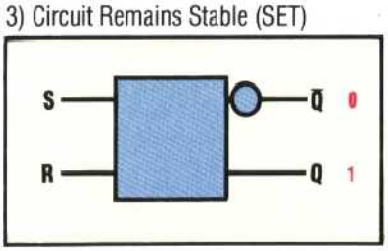



2) A Pulse On The SET Line



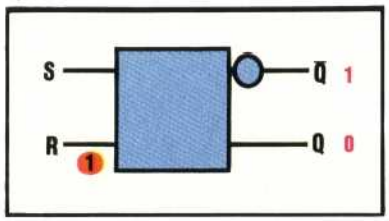

When the input pulse on the S line ceases, the circuit remains in a stable SET state.

3) Circuit Remains Stable (SET)




A pulse sent along the R line flips (flops) the circuit back to its original RESET state.

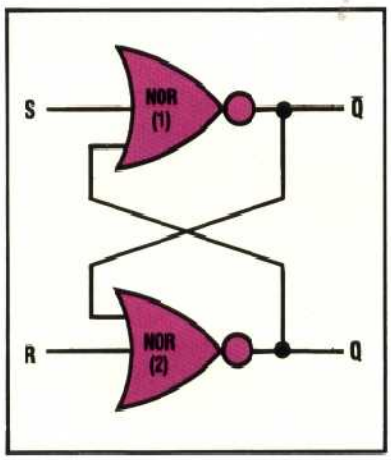
4) A Pulse On The RESET Line




Having now described the function of an R-S flip-flop, let's take a closer look at the logic elements in the circuit.

## R-S FLIP-FLOP CIRCUIT

An R-S flip-flop can be constructed using several techniques, such as linking two NAND gates together, or, as in our example here, by linking two NOR gates together so that the output from each gate forms one of the inputs to the other. It is this 'looping back' of the logic signals that gives the flip-flop its 'memory' capacity.




Let us then trace the SET and RESET functions of the flip-flop and see how they are achieved by this combination of NOR gates. If we assume that initially the flip-flop is in the RESET state and there are no input pulses then the circuit will be in a stable state. (Remember that a NOR gate only gives an output of one if both inputs are zero.) A pulse along the S line will upset this stable arrangement causing the 'not Q' ($\overline{Q}$) output to change to zero. This affects the 'looped-back' input to the second NOR gate (2), causing the output from that gate, Q, to change to one. This in turn means that if the pulse is still present on the first NOR gate (1), then the inputs to NOR gate(1) will both be one. Thus, the output from NOR gate(1) will still be zero and so the circuit has reached a stable state, i.e. it is SET.